U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,271,110 (Yamaguchi et al.) or U.S. Patent No. 5,592,736 (Akram et al.) or JP Patent No. 08-191072 (Takahiro et al.) in view of U.S. Patent No. 5,643,831 (Ochiai et al.) and JP Patent No. 05206221 (Michihiko et al.).

By the present response, Applicants have submitted a new title of the invention. Claims 34-53 remain pending in the present application.

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Applicants note that the Examiner has failed to supply Applicants with a copy of the Notice of References Cited and respectfully request that a copy of this be sent to Applicants with the next Office Action.

New Title Requirement

The Examiner asserts that the title of the invention is not descriptive and, therefore, has required a new title. Applicants have submitted a new title of the invention to comply with the Examiner's request.

35 U.S.C. §103 Rejections

Claims 34-53 have been rejected under 35 U.S.C. §103(a). Applicants respectfully traverse these rejections.

Yamaguchi et al. discloses bump-forming method using two plates and an electronic device where first and second ball-forming plates are prepared. The cavities of the first plate and the cavities of the second plate are filled with solder paste, respectively. The first plate and the second plate are placed in a facing relationship to each other and heated to form metal balls each of which corresponds to the total metal components of the solder paste in one cavity of the first plate and one cavity in the second plate. The metal balls are formed in the cavities of the lower plate. The metal balls are transferred from the cavities of the first plate to a device on which bumps are to be formed.

Akram et al. discloses a method for testing unpackaged semiconductor dice having raised contact locations (e.g., bumped bond pads) and a method for forming

an interconnect suitable for testing this type of dice. The interconnect includes a substrate having contact members having an array of sharpened elongated projections. The sharpened projections are formed by etching (or by growing and removing an oxide) through exposed areas of a mask. A conductive layer is formed on the sharpened projections and is in electrical communication with conductive traces formed on the substrate. The sharpened projections are adapted to penetrate the contact location on the die to a limited penetration depth to establish an ohmic connection while minimizing damage to the contact location.

Takahiro et al. discloses a terminal electrode structure of thin film circuit element where conductive resin terminal parts are arranged on pads formed at terminal arrangement positions of a thin film circuit element to realize cost reduction and improve conventional restrictions in the size and accuracy.

Ochiai et al. discloses a method for fabricating a semiconductor device using a solder ball-forming plate having cavities. The plate is made from a silicon plate having a flat surface and a crystallographic plane, and an orientation flat in a crystallographic plane. The cavities are formed on the flat surface of the plate by etching, using a mask having openings in the shape of rhombus arranged such that one side of the rhombus is generally parallel to the crystallographic plane. The cavities having wedge-shaped bottom are then formed as a result. The cavities are then filled with a solder paste and are then heated to form solder balls in the cavities while the plate is in an inclined position. The solder balls are then transferred from the plate to a semiconductor chip.

Michihiko et al. discloses a connection structure of an IC chip that prevents generation of short circuits between adjacent solder bumps when the pitch of the IC chip electrodes is fine. When thermal compression bonding is performed at a heating temperature wherein the solder layer is fused but the solder bump is not fused, the barrel type solder part is not crushed in the lateral direction but the cone type solder part is suitably crushed via the solder layer by a metal bump. Thereby the solder bump is not stretched in the lateral direction as a whole so that short

the claims of the present application.

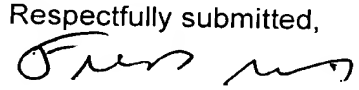
Regarding claims 35-52, Applicants submit that these claims are dependent on independent claim 34 and, therefore, are patentable at least for the same reasons noted regarding this independent claim. For example, none of the cited references, taken alone or in combination, disclose plating gold on the metal filled by plating or the surface of a protruded electrode being plated with gold after the transfer.

Accordingly, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose suggest or render obvious the limitations in the combination of each of claims 34-53 of the present application. Applicants respectfully request that these rejections be withdrawn and that these claims be allowed.

In view of the foregoing amendments and remarks, Applicants submit that claims 34-53 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees and excess claim fees, to Deposit Account No. 01-2135 (referencing case No. 500.38090X00) and please credit any excess fees to such deposit account.

Respectfully submitted,



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US 094627960RP1

Creation date: 01-20-2004
Indexing Officer: WMICHAEL - WORKHA MICHAEL
Team: OIPEBackFileIndexing
Dossier: 09462796

Legal Date: 10-07-2003

No.	Doccode	Number of pages
1	CTNF	6
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Total number of pages: 34

Remarks:

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